UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,342	07/09/2003	Vincent Chan	00100.66.0068	1507

23418 7590 05/18/2004

VEDDER PRICE KAUFMAN & KAMMHOLZ
222 N. LASALLE STREET
CHICAGO, IL 60601

EXAMINER	
ROMAN, ANGEL	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,342	CHAN ET AL.	
	Examiner	Art Unit	
	Angel Roman	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-45* is/are pending in the application.

4a) Of the above claim(s) *29,30,34 and 38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27,28,31-33,35-37 and 40-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Specie I in Paper No. 02172004 is acknowledged. The traversal is on the ground(s) that the examiner has not provided any indication as to which claims provide for each asserted species and that independent claims 27 and 43 are represented by figures 6 and 9. This is not found persuasive because it is the Applicants burden to list all the claims readable on the elected specie, as clearly indicated in the previous election of species requirement. Regarding claims 27 and 43 the Examiner asserts that this claims are generic claims represented by figures 6 and 9 and upon allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include limitations of an allowed generic claim as provided by 37 CFR 1.141.

The requirement is still deemed proper and is therefore made FINAL.

Applicants indicated that claims 27-45 are directed to the specie illustrated in figure 6, however dependent claims 29, 30, 34 and 38 claim features not directed to the specie illustrated in figure 6 and are not being considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 27, 32, 33 and 41-44 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanioka U.S. Patent 5,784,264 A.

Tanioka discloses a method comprising; directly attaching a first semiconductor die 2 to a package/module substrate 19; forming electrical connections 15 (wire-bonding) between the first semiconductor die 2 and the package/module substrate 19; securing the electrical connections by using a rectangular encapsulation 16; placing a second semiconductor die in a die package 17; attaching the die package to the package/module substrate 19 and forming electrical connections between the die package and the package substrate (see figure 2A). The encapsulation 16 having a planar top surface equidistantly from a surface of the package/module substrate with a second semiconductor die package top surface.

4. Claims 27, 28, 32, 33, 35, 37, and 42-45 rejected under 35 U.S.C. 102(e) as being clearly anticipated by Watanabe et al. U.S. Patent Application Publication 20020074669 A1.

Watanabe et al. discloses a method for packaging semiconductor devices comprising; directly attaching a first semiconductor die 4B to a package/module substrate 2; forming wire bond electrical connections 7 between the first semiconductor die 4B and the package/module substrate 2; securing the electrical connections 7 by forming a rectangular encapsulation 8 over the die 4B; placing a second semiconductor die in a die package 4A; attaching the die package to the package/module substrate 2; and forming ball grid array electrical connections 5 between the die package and the package/module substrate 2 (see figure 11). Watanabe et al also discloses attaching solder balls 3 to an underside of the package/module substrate 2 and attaching a heat sink 16 to the package/module substrate 16. The encapsulation 8 having a planar top surface equidistantly from a surface of the package/module substrate with a second semiconductor die package top surface (see figure 12).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka U.S. Patent 5,784,264 A in view of Fallon et al. U.S. Patent 5,872,051 B1.

Tanioka discloses the subject matter applied above but lacks anticipation in disclosing that the chip 2 is attached using adhesives. Fallon et al. discloses attaching a semiconductor die 924 to a package substrate using adhesive 938. In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use adhesives to secure the semiconductor die to the package substrate in the primary reference of Tanioka as disclose in Fallon et al. in order to provide mechanical stability to the semiconductor chip.

9. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka U.S. Patent 5,784,264 A in view of Takano et al. U.S. Patent 6,376,907 B1.

Tanioka is applied as above but lacks anticipation on disclosing standard package sizes being 40mm X 40mm. Takano et al. teaches a standard package sizes being 40mm X 40mm (see TABLE 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Tanioka by using the standard package sizes as taught by Takano et al. in order to reduce limitation in the size of the semiconductor chip (see column 2, lines 6 and 7).

10. Claims 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanioka U.S. Patent 5,784,264 A in view of Shinonaga et al. U.S. Patent Application publication 20020025608 A1.

Tanioka is applied as above but lacks anticipation on testing the die package and the semiconductor die prior to attaching them to the package substrate. Shinonaga et al. discloses testing chips prior to mounting the chips on a package substrate (see Abstract). In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to test the die package and the semiconductor die in the primary reference of Tanioka prior to mounting them on the package substrate as disclosed in Shinonaga et al. since it would reduce process costs.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Brillhart, Otani, Najafi et al., Giussani, Bernier et al. and Ozawa disclose methods for packaging semiconductors on package substrates.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (571) 272-1681. The examiner can normally be reached on Monday-Friday 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800

AR
May 2, 2004